

What is claimed is:

1. A program logic device comprising:

a control processor operating according to a high speed clock, the high speed clock obtained by multiplying a standard
5 clock;

input means for inputting signal information into the control processor; and

output means for outputting the signal information of the control processor as a signal, wherein

10 while the control processor is executing a plurality of processings according to the high speed clock, control is determined according to the signal captured by the input means synchronously with the standard clock within one cycle and a value of the output means is changed by the control.

15 2. A program logic device comprising:

a control processor operating according to a high speed clock, the high speed clock obtained by multiplying a standard clock;

20 input means for inputting signal information into the control processor; and

output means for outputting the signal information of the control processor as a signal, wherein

25 while the control processor is executing a plurality of processings according to the high speed clock, control is determined according to a value of the signal captured by the input means synchronously with the standard clock within a

plurality of cycles of the standard clock and a value of the output means is changed by the control.

3. A program logic device according to claim 1, wherein
5 the value of said output means is changed synchronously with said standard clock.

4. A program logic device according to claim 1, wherein
10 said control processor has a delay function to synchronize with said standard clock and conducts a next processing after waiting for a predetermined transition of the standard clock.

5. A program logic device according to claim 1, wherein
15 the control conducted by said control processor is determined according to the value of the signal captured by said input means synchronously with said standard clock.

6. A program logic device according to claim 1, wherein
20 the program logic device comprises:
comparison value storage means for storing a predetermined comparison value in advance; and

a comparator for comparing the comparison value with the value of the signal captured by said input means synchronously with said standard clock, and wherein

25 a control content of said control processor is determined according to a comparison result of the comparator.

7. A program logic device according to claim 1, wherein the program logic device comprises:

comparison value storage means for storing a predetermined comparison value in advance;

5 preprocessing means for performing an arithmetic operation of the value of the signal captured by said input means synchronously with said standard clock, and for setting the value of the signal; and

10 comparison means for comparing the comparison value with the value set by the preprocessing means, and wherein a control content of said control processor is determined according to a comparison result of the comparator.

8. A program logic device according to claim 1, wherein

15 after waiting for the value of the signal captured by said input means synchronously with said standard clock to become a predetermined value, the control set by the predetermined value is conducted.

20 9. A program logic device according to claim 8, wherein

a wait state is released when the number of cycles of said standard clock reaches a predetermined number after the wait state.

25 10. A program logic device according to claim 8, wherein

a wait state is released by controlling said control processor for itself.

11. A program logic device according to claim 8, wherein
a wait state is released when the value of the signal
captured by said input means becomes a predetermined value.

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12. A program logic device according to claim 1, wherein
an interrupt synchronous with the standard clock is
generated to said control processor according to the value of
the signal captured by said input means synchronously with said
standard clock.

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13. A program logic device according to claim 1, wherein
the program logic device comprises:

comparison value storage means for storing a predetermined
comparison value in advance; and

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a comparator for comparing the comparison value with the
value of the signal captured by said input means synchronously
with said standard clock, and wherein

an interrupt synchronous with the standard clock is
generated to said control processor according to a comparison
result of the comparator.

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14. A program logic device according to claim 1, wherein
the program logic device comprises:

comparison value storage means for storing a predetermined
comparison value in advance;

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preprocessing means for performing an arithmetic

operation of the value of the signal fetched by said input means
synchronously with said standard clock, and for setting the value
of the signal; and

5 a comparator for comparing the comparison value with the
value of the signal set by the preprocessing means, and wherein
an interrupt synchronous with the standard clock is
generated to said control processor.

10 15. A program logic device according to claim 12, wherein
an interrupted position in said control processor is
changed according to a comparison result of said comparator.